DRONACHARYA
College of Engineering

KHENTAWAS, FARRUKHNAGAR, GURGAON, HR

Department:

Academic Session: 2017-18 (Jan-June 2018)

Lesson Plan for the Semester started w.e.f 08.01.2018

Subject with code:COMPUTER ARCHITECTURE & ORGANIZATION

Name of Faculty with designation : SAMEEKSHA KUKRETI

Month	Date & Day	Sem-Class	Unit	Topic/Chapter covered	Academic activity	Test / assignment
January	09.01.2018 Tuesday	IV-CSE-II,CSIT,ECS	1	Boolean algebra and Logic gates	....	Assignment of 02 Ques. given
January	10.01.2018 Wednesday	IV-CSE-II,CSIT,ECS	1	Combinational logic blocks(Adders, Multiplexers, Encoders, de-coder),		Assignment of 02 Ques. given
January	12.01.2018 Friday	IV-CSE-II,CSIT,ECS	1	Sequential logic blocks(Latches, Flip-Flops, Registers, Counters) Store program control concept		Assignment of 02 Ques. given
January	16.01.2018 Tuesday	IV-CSE-II,CSIT,ECS	1	Flynn's classification of computers (SISD, MISD, MIMD)		Assignment of 02 Ques. given
January	17.01.2018 Wednesday	IV-CSE-II,CSIT,ECS	1	Multilevel viewpoint of a machine: digital logic, micro architecture		Assignment of 02 Ques. given
January	19.01.2018 Friday	IV-CSE-II,CSIT,ECS	1	ISA, operating systems		Assignment of 02 Ques. given
January	23.01.2018 Tuesday	IV-CSE-II,CSIT,ECS	1	High level language; structured organization; CPU, caches,		Assignment of 02 Ques. given

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January	24.01.2018 Wednesday	IV-CSE-II,CSIT,ECS	1	Main memory, secondary memory units & I/O; Performance metrics; MIPS, MFLOPS.		Assignment of 02 Ques. given
January	30.01.2018 Tuesday	IV-CSE-II,CSIT,ECS	2	Instruction set based classification of processors (RISC, CISC, and their comparison)		Assignment of 02 Ques. given
February	02.02.2018 Friday	IV-CSE-II,CSIT,ECS	2	Addressing modes: register, immediate, direct, indirect, indexed; Operations in the instruction set		Assignment of 02 Ques. given
February	06.02.2018 Tuesday	IV-CSE-II,CSIT,ECS	2	Arithmetic and Logical, Data Transfer, Control Flow		Assignment of 02 Ques. given
February	07.02.2018 Wednesday	IV-CSE-II,CSIT,ECS	2	Instruction set formats (fixed, variable, hybrid);		Assignment of 02 Ques. given
February	09.02.2018 Friday	IV-CSE-II,CSIT,ECS	2	Language of the machine: 8086 ; simulation using MSAM.		Assignment of 02 Ques. given
February	20.02.2018 Tuesday	IV-CSE-II,CSIT,ECS	3	CPU Architecture types (accumulator, register, stack, memory/ register)		Assignment of 02 Ques. given
February	21.02.2018 Wednesday	IV-CSE-II,CSIT,ECS	3	Register based CPU, Fetch-Decode-Execute cycle (typically 3 to 5 stage)		Assignment of 02 Ques. given
February	23.02.2018 Friday	IV-CSE-II,CSIT,ECS	3	Microinstruction sequencing		Assignment of 02 Ques. given
February	27.02.2018 Tuesday	IV-CSE-II,CSIT,ECS	3	Implementation of control unit, The need for a memory hierarchy.		Assignment of 02 Ques. given
February	28.02.2018 Wednesday	IV-CSE-II,CSIT,ECS	3	Pipelining(Enhancing performance with pipelining)		Assignment of 02 Ques. given
March	06.03.2018 Tuesday	IV-CSE-II,CSIT,ECS	3	Cache, main memory and secondary memory		Assignment of 02 Ques. given

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March	07.03.2018 Wednesday	IV-CSE-II,CSIT,ECS	3	Memory parameters: access/ cycle time, cost per bit); Main memory (Semiconductor RAM & ROM organization,		**Assignment of 02 Ques. given**
March	09.03.2018 Friday	IV-CSE-II,CSIT,ECS	3	**Memory expansion, Static & dynamic memory types)**		**Assignment of 02 Ques. given**
March	13.03.2018 Tuesday	IV-CSE-II,CSIT,ECS	3	**Cache memory (Associative & direct mapped cache organizations.**		**Assignment of 02 Ques. given**
March	14.03.2018 Wednesday	IV-CSE-II,CSIT,ECS	4	Goals of parallelism (Exploitation of concurrency, throughput enhancement); Amdahl's law		**Assignment of 02 Ques. given**
March	16.03.2018 Friday	IV-CSE-II,CSIT,ECS	4	Instruction level parallelism (pipelining, super scaling –basic features)Processor level parallelism.		**Assignment of 02 Ques. given**
March	27.03.2018 Tuesday	IV-CSE-II,CSIT,ECS	4	Instruction codes, computer register, computer instructions, timing and control reference instruction cycle		**Assignment of 02 Ques. given**
March	28.03.2018 Wenesday	IV-CSE-II,CSIT,ECS	4	Type of instructions, memory reference, register reference		**Assignment of 02 Ques. given**
April	03.04.2018 Tuesday	IV-CSE-II,CSIT,ECS	4	Memory Hierarchy I/O reference, accumulator logic, Control memory		**Assignment of 02 Ques. given**
April	04.04.2018 Wednesday	IV-CSE-II,CSIT,ECS	4	Instruction Formats, Types of interrupts.		**Assignment of 02 Ques. given**
April	06.04.2018 Friday	IV-CSE-II,CSIT,ECS		Micro-instruction formats, micro-program sequencer, Stack Organization.		
April	10.04.2018 Tuesday	IV-CSE-II,CSIT,ECS		revision		